CLAIMS

1. A method of communicating between a MAC and a PHY comprising:

sending a 100 MHz time-division multiplexed signal on a receive data line ;

sending a time-division multiplexed receive control signal on a receive control line;

sending a 100 MHz time-division multiplexed signal on a transmit data line;

sending a time-division multiplexed transmit control signal on a transmit control line.

2. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

3. A method of communicating between a MAC and a PHY as recited in claim 2 wherein the receive data line includes 4 bit segments and wherein the beginning of a 4 bit segment is determined by the synchronization bit.

4. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a receive data valid bit.

5. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and wherein each 4 bit segment includes a receive error bit.

6. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed receive control signal includes 4 bit segments and ~~wherein each 4 bit segment includes a carrier sense bit.~~

7. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a synchronization bit.

8. A method of communicating between a MAC and a PHY as recited in claim 7 wherein the transmit data line includes 4 bit segments and wherein the beginning of a 4 bit segment is determined by the synchronization bit.

9. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a transmit enable bit.

10. A method of communicating between a MAC and a PHY as recited in claim 1 wherein the time-division multiplexed transmit control signal includes 4 bit segments and wherein each 4 bit segment includes a transmit error bit.

11. A method of communicating between a MAC and a PHY as recited in claim 1 further including indicating the speed of the PHY using the receive data line.

12. A method of communicating between a MAC and a PHY as recited in claim 11 wherein indicating the speed of the PHY using the receive data line includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error.

13. A method of communicating between a MAC and a PHY as recited in claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long.

14. A method of communicating between a MAC and a PHY as recited in claim 1 further including buffering data transmitted from the PHY to the MAC using an elasticity buffer that long enough to buffer an entire frame of data from a data source ~~having a clock with a frequency tolerance of 0.1%.~~

15. An interface between a first MAC and a second MAC consisting essentially of:

a time-division multiplexed receive data line;

a time-division multiplexed receive control line;

a time-division multiplexed transmit data line;

a time-division multiplexed transmit control line.

16. A MAC to PHY interface consisting essentially of:

a common clock;

a time-division multiplexed receive data line;

a time-division multiplexed receive control line;

a time-division multiplexed transmit data line;

a time-division multiplexed transmit control line.